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Claims

[c1] What is claimed is:

1.A method of defect control of a semiconductor process comprising following steps:

providing a patterned wafer comprising a plurality of first defects;

performing a semiconductor process which forms a plurality of second defects on the patterned wafer;

performing a defect inspection to detect the plurality of first defects and second defects; and

classifying the detected defects into the first defects and the second defects and separating the second defects into a plurality of defect types according to a predetermined database.

[c2] 2.The method of claim 1 wherein the database comprises a classifying rule of each defect type and defect information of each defect type.

[c3] 3.The method of claim 2 wherein the defect information of each defect type comprises an influence degree over a yield of the semiconductor process of each defect type.

[c4] 4.The method of claim 3 wherein the method further

separates the second defects into killer defects and non-killer defects according to the degree of the influence degree over the yield of the semiconductor process after classifying the defects.

[c5] 5.The method of claim 4 wherein when killer defects are detected, the method further comprises following steps:
performing a root cause analysis according to the defect type of the detected defects; and
informing a responsible person of the semiconductor process to correct process parameters of the semiconductor process.

[c6] 6.The method of claim 1 wherein the method utilizes in-line automatic defect classification (ADC) tools to classify the defects.

[c7] 7.The method of claim 1 wherein the patterned wafer is an in-line product wafer.